

# Mapping Leakages on USJ Test Wafers

James T C Chen, Tatiana Dimitrova and Dimitar Dimitrov

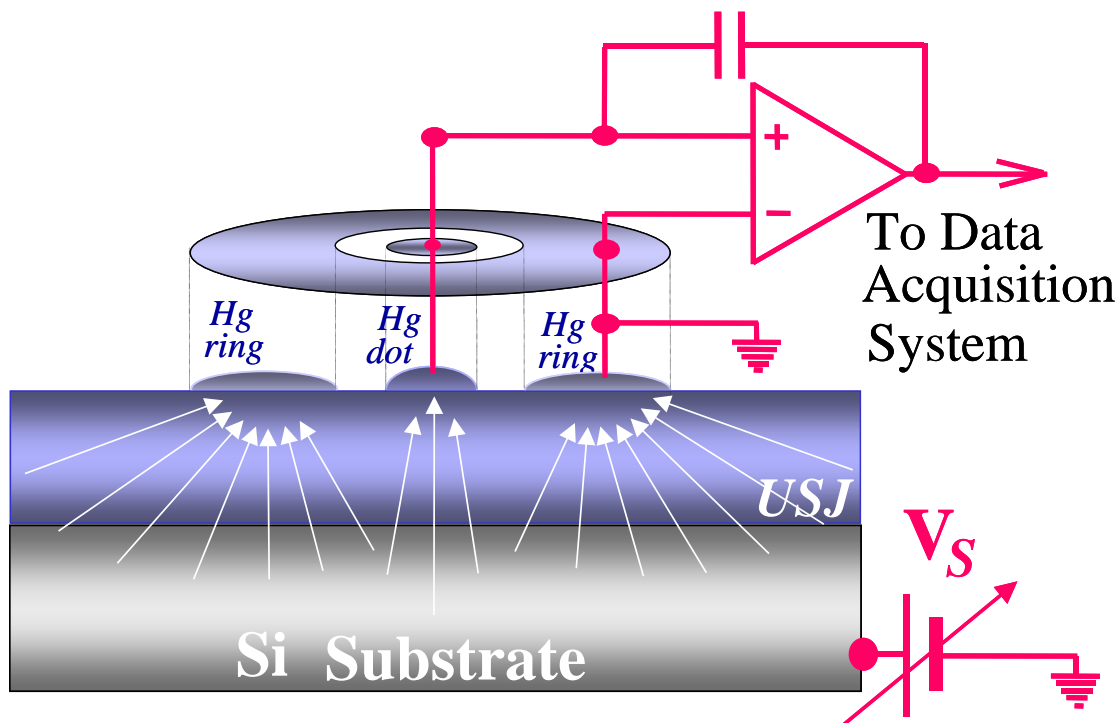
*Four Dimensions, Inc.,*

*3140Diablo Ave, Hayward, California 94545*

Email: [infor@4dimensions.com](mailto:infor@4dimensions.com)

Tel: (510) 782-1843, Fax: 510) 786-9321

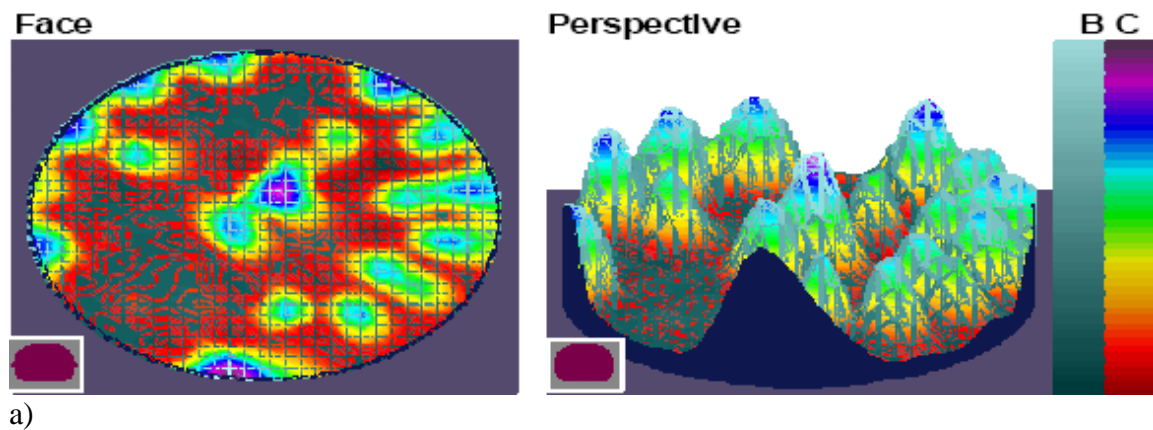
It is well recognized that making the leakage in the 45nm node and further advanced ICs to be within an acceptable limit is difficult but of vital important to the reliability. Also, in such kind of devices, the areas of source and drain are much bigger than the gate areas. Therefore, monitoring the USJ leakage for process control in IC fabrication should be very important.

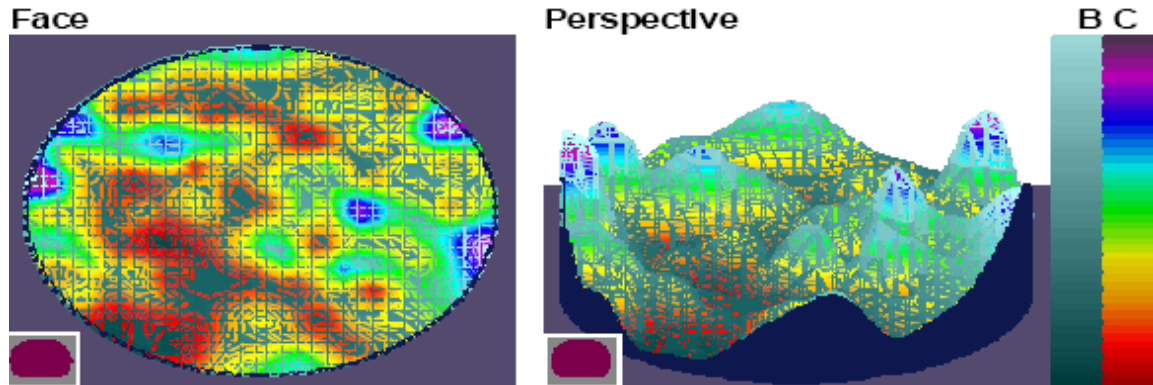


**Fig.1.** Schematic representation of the USJ leakage current distribution (symbolized by arrows) under mercury dot-ring electrodes and how the leakage current around the dot is measured.

Methods for monitoring USJ leakage using test wafers have been proposed by Chen & Liu [1] and Faifer et al.[2]. However, the former method requires a masking step although it should result in more accurate measurement than other methods; the latter, although is a non-contact method, is based on a formula with much simplification in its deriving and relying on such kind of surface voltage measurements that is hard to be accurate. This formula also requires knowledge of the parameters hard to obtain accurately, and the leakage current it refers to is recombination current, not junction leakage current at a reversely biased voltage.

We are proposing a new method for measuring and mapping leakage of non-patterned USJ under bias. The method employs an automatic mercury dot-ring probe, with the dot connected to an ground potential integrator and the ring grounded, to probe the USJ layer on a wafer whose substrate is biased at  $V_s$  through the chuck, as shown in Fig. 1. In this connection, the substrate bias will cause current to flow through the junction towards the dot and ring, depending on the bias. But only the junction current at immediate under and at close proximity of the dot will be taken by the integrator, while the junction current from the other areas should be collected by the ring. Thus I-V curve can be plotted with good geometric resolution and maps of leakage current can be made for various bias. Figs. 2(a) and (b) show contour and 3D maps of USJ leakage on a wafer under 1V bias. The maps clearly reflect pattern of annealing sweeps by revealing the regions of high defect density of the USJ. The effective area of leakage current collected by the integrator is estimated to be about one order of magnitude larger than the dot area, which is  $0.00804 \text{ cm}^2$ .





b)

**Fig.2.** USJ leakage current distribution in a 300 mm Si wafer. Contour and 3D maps are shown for a case of IV reverse bias between the Hg dot and the Si substrate.

We intend to use the automatic mercury probe to study the effects of various implantation processes, annealing processes and background doping level to the USJ leakage and its pattern, from samples available to us, for presenting to the workshop.

[1]. J.T.C. Chen and W. Liu, Using Mercury Probes to Characterize USJ Layer, USJ 2005, Dayton Beach, Florida, USA, pp.103-108.

[2]. V.N. Faifer et al., "Non-Contact Electrical Measurements of Sheet Resistance and Leakage Current Mapping for Ultra-Shallow (and Other) Junctions," MRS-Spring 2004 Symp. C, Vol. 810, p. 475.